2021 20th International Symposium on Distributed Computing and Applications for Business Engineering and Science (DCABES)

A High Precision Refresh Method to Improve The Performance of Flash Storage Devices

Peixuan Li[1,2,3,4], Yaofang Zhang[1,2,3,4], Deli Yin[5], Ping Xie[1,2,3,4*]

1.College of Computer of Qinghai Normal University, Xining 810016, P. R. China
2.The State Key Laboratory of Tibetan Intelligent Information Processing and Application, Xining 810016, P. R. China
3.The Key Laboratory of Internet of Things of Qinghai Province, Xining 810016, P. R. China
4.Academy of Plateau Science and Sustainability, Xining 810016, P. R. China
5.Chuzhou Polytechnic, Chuzhou, 239000, P. R. China
**Corresponding author: xieping@qhnu.edu.cn*

***Abstract*—With the development of flash memory, its storage density has gradually increased, but its reliability has been greatly reduced. Now, flash memory relies on LDPC to solve this problem. Although LDPC (Low Density Parity Check Code) can correct data with a high error rate, it will cause a lot of delays. The refresh operation can cause the LDPC decoding delay. In the work of this article, we propose a precise refresh strategy. On the basis of high latency pages, according to the characteristics of data access frequency, we take the read-hot data in the write-cold data as our refresh target. We test the performance of the precise refresh scheme through different workloads. Compared with ordinary refresh schemes, the average response time of flash memory storage devices is reduced by 16%-49% and the lifetime of flash memory is extended.**

Keywords-LDPC, refresh, Nand flash, hot data

I. INTRODUCTION

Nowadays, SSD (Solid State Drive) with flash memory as storage media are very popular in computer systems and mobile devices. It has the advantages of fast reading speed, small size, lightweight, etc. In consumer products, MLC/TLC (multi-level/three-level cell) flash memory chips that store 2 or 3 bits per cell are used[1][2]. Although the cost price is gradually decreasing but the capacity is gradually increasing. And the storage density is higher. As storage density increases, devices need more precise voltage control capabilities when reading data. In addition, because multiple bits are compressed into one unit, the fault tolerance of the flash memory is lower, and voltage changes are more likely to cause errors in the flash memory. The improvement of the error rate of flash memory makes the error correction capability of the traditional BCH (Bose Chaudhuri Hocquenghem) error correction code no longer suitable for solid state drives composed of high-density flash memory. Nowadays, the design of LDPC in solid-state hard drives is continuously being applied in practice[3][4].

LDPC provides a strong reliability guarantee for flash storage devices. LDPC uses an iterative way to decode. The purpose of decoding iteration is to accumulate bit decision information. The more iterations, the higher the reliability of the bit decision. It can be used to correct higher error rate data, but it will also cause a lot of error correction delays. Due to the current situation of high latency, two optimization methods are now proposed. The first way is to speed up LDPC decoding. It reduces the decoding waiting time by caching all kinds of LDPC information[5] or providing additional decision information[6] to the decoding process. The second is to reduce the data error rate. The method is to correct the error of the data and write to a new location when the error rate of the data exceeds a certain security level[7]. Although the data error rate is reduced, it has serious shortcomings. Because it will cause additional reading, programming, and erasing operations, thereby affecting the performance and lifetime of flash memory storage.

In order to reduce the negative impact of LDPC and refresh, this work proposes a precise refresh plan. The basic idea is that the refreshed framework uses periodic refresh to refresh high-latency pages that have write-cold attributes and read-hot attributes. Therefore, we need to analyze the attributes of the flash memory pages and define high-latency data. According to previous research, the reading level of LDPC is 1-7[8]. The higher the reading level, the higher the decoding accuracy and the greater the delay. We found that when the reading level of LDPC is higher than a certain threshold, its decoding delay increases significantly. In a refresh cycle, if a logical data page is written less than twice, it is a write-cold data page if it is read more than twice, it is a read-hot data page. The above scheme is implemented in a well-configured flash simulator. Experiments with several actual workloads show that the refreshed framework can improve the average response time of the device while ensuring the lifetime of the flash memory.

II. BACKGROUND AND MOTIVATION

A. LDPC Encode and Decode

When executing a read request, the SSD controller always performs LDPC decoding on the flash memory first, and then returns the error-corrected data to the host. LDPC decoding always starts with hard decision decoding. When hard decision decoding fails, LDPC will perform soft decision decoding. Soft decision decoding has strong error correction capability and fast convergence speed, but it has a large number of calculations and high hardware overheads. Because soft decision decoding will go through three steps[9]:

2473-3636/21/$31.00 ©2021 IEEE
DOI 10.1109/DCABES52998.2021.00060

1) Reread operation: The reread operation reads one or more sets of data in the flash memory according to the way the soft data is constructed, which can obtain multiple sets of information useful for decoding.

2) Soft data construction: The reread operation will read out multiple groups of different information about flash memory data composed of "0" and "1". LDPC will map these information into soft data that can be decoded by LDPC decoding. Each bit of data has a LLR(Log Likelihood Ratio).

3) Perform soft decision decoding: After constructing the soft data, each LLR in the codeword is passed to the LDPC decoder. Each real number in the LLR represents the probability of each bit of data "0" and "1". A positive number represents a greater probability of "0", and a negative number represents a greater probability of "1". In this way, the mistake of flash memory can be corrected.

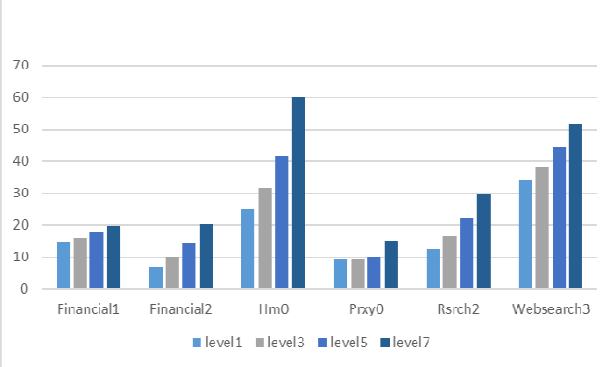

Figure 1. Refresh the framework

We use experiments to show the average access latency under different decoding levels, as shown in Figure 1. As the LDPC reading level increases, the average response delay of the device gradually increases. From level 5 to level 7, the average response delay of Financial2 increased by 39%, and Hm0 increased by 32%. When the LDPC reading level is 5, the average response time of the device has increased significantly, indicating that more LDPC decoding delays have occurred.

B. *Read-hot and Write-hot Data*

The hot or cold data is determined by the frequency of access. Read-hot data refers to data that has been accessed more frequently and read-cold data refers to data that has less access times. Identifying hot and cold data can effectively improve the performance of flash storage algorithms. Hot data recognition technology is used to reduce write amplification, improve garbage collection performance[10][11][12], etc. Not only read operations can affect data, but write operations also affect data. On different pages, the write frequency may be quite uneven. Some pages may be frequently written (write-hot pages), other pages are rarely updated (write-cold pages). The data written to the cold page is not updated frequently, and a large number of retention errors will occur, resulting in increased read latency. The write-hot page usually only has a low bit error rate. Even if the bit error rate is high, the page will be overwritten by new data due to the high update probability. The benefit of refreshing write-hot pages is low. So the benefit of refreshing cold pages is higher. Write-hot data only accounts for 1% of the total data[13], so accurate refresh still needs further analysis. At the same time, if a cold read page is refreshed, the system will no longer access the page. Then we only have the loss of refresh, but no gain. According to the popularity of the data, we propose a precise refresh plan.

III. ACCURATE REFRESH SCHEME

A. *Flash Refresh Framework*

In this section we introduced the design of the precise refresh framework, as shown in Figure 2. The address mapping module maintains the correspondence between the logical page address and the physical page address for the system. The refresh framework can get the basic information of all pages from the address mapping module. The ECC (Error Correcting Code) module provides decoding delay information for the refreshed frame. Determine whether it is a high-latency page according to the LDPC decoding level of the flash page. The refresh strategy proposed in this paper is to determine whether to refresh the high-latency page based on the write heat and read heat information of the flash memory page. The hot data judgment module will provide corresponding information for the refresh strategy. Every time interval, all data blocks that meet the refresh conditions will be refreshed to ensure data reliability. This scheme will be discussed in detail below.

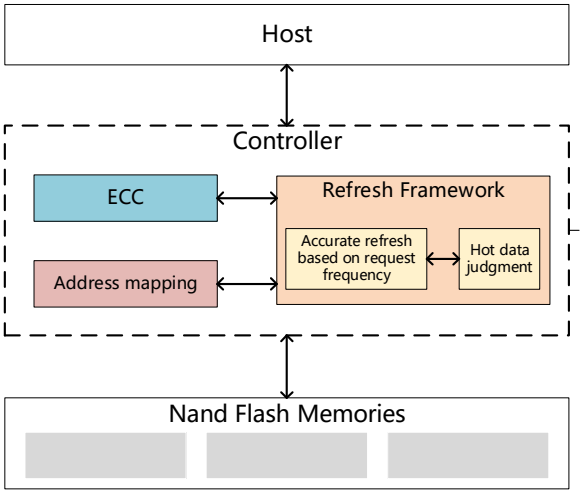

Figure 2. Refresh the framework

B. *Hot Data Judgment Module*

We have designed two queues, one is used to judge the hot read data page, the other is used to judge the hot write data page. When a data page is read for the second time, the address information of the flash memory page will be put into the hot read data queue. The hot data queue has limited storage space. If the hot read data has not been accessed for a long time, it will leave the hot read queue and become cold read data again. The same method can be used to determine the write-hot data page. After a cycle is refreshed, both queues will be emptied and the hot data will be judged again.

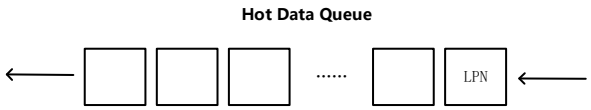

Figure 3. The process based on the high LDPC delay block refresh policy

C. *Accurate Refresh Based on Heat*

The accurate refresh based on heat scheme determines the high latency page to be refreshed according to the write heat and degree heat of the page, figure 4 shows the process of the high-precision refresh scheme. In a refresh cycle, the framework calculates the read frequency, write frequency, and LDPC error correction delay of flash memory pages. In the second chapter, we show through load experiments that the delay increases when LDPC decoding level 5 is greater. Therefore, pages with LDPC decoding levels above level 5 are high-latency pages. If the flash memory has been written (read) data more than twice, the page is read-hot (write-hot) data. If the data stored in a high-latency flash page is both write-cold data and read-hot data, the data page is refreshed. The heat information of the data is given by the heat data judgment module.

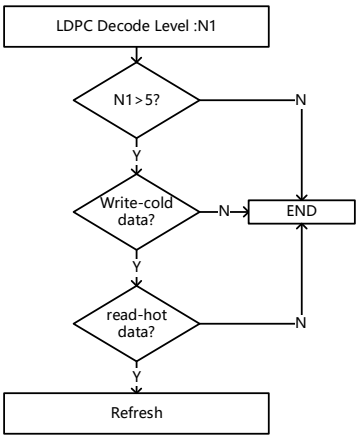

Figure 4. The number of grades above 3 level and above 5 level within the block mark the update process.

IV. EXPERIMENTTAL ANALYSIS

In this section, we show the basic configuration of the experimental device and flash memory storage device. Test the effect of refresh strategy through workload experiments. The impact of the refresh strategy on the average response time and lifespan of flash storage devices is analyzed.

A. *The Experimental Device*

We added Microsoft's SSD module to DiskSim[14] to simulate flash storage devices. The storage device is configured with 8 channels, each channel has 8 chips, each chip has 4 planes, each plane has 2048 blocks, each block has 64 8KB pages and the LDPC software decode read level is set to 1-7. In terms of workloads, eight workloads with different read/write ratios were used to test the effect of the refresh strategy based on high LDPC delay blocks. We listed the information for each load, as shown in Table 1.

TABLE I. WORKLOAD INFORMATION

Workload	Read	Write	Read ratio
Financial1	1235633	4099353	23%
Mds0	143973	1067061	12%
Prxy0	383524	12135444	3%
Hm0	1417748	2575568	37%
Rsrch2	136364	71223	65%
Financial2	3046112	653082	82%
Proj0	13006718	1907336	87%
Websearch3	16410267	26772	98%

During the experiment, we evaluated four strategies:

1) The original strategy: In the original strategy, the flash storage device does not have the refresh capability and only relies on the device's garbage collection module, ECC module and wear balance module to ensure the reliability of data..

2) Traditional refresh strategy: In the traditional refresh strategy, datas are refreshed only when the data error rate reaches the threshold that cannot be corrected by the ECC module.

3) The Accurate refresh strategy: This is the refresh strategy proposed in this article. Refresh high latency pages according to the characteristics of write heat and read heat.

B. *Experimental results and analysis*

In this section, we analyzed the average response time and the number of refreshes for precise refresh.

Figure 5 shows the normalized average response time of the three strategies. The precise refresh scheme reduces the average response time of the workload to a certain extent. The higher the read ratio, the more read-hot data. The optimization of precise refresh to read latency is more obvious. For loads with a reading ratio of more than 50%, their average response time is reduced by 16% to 49%.

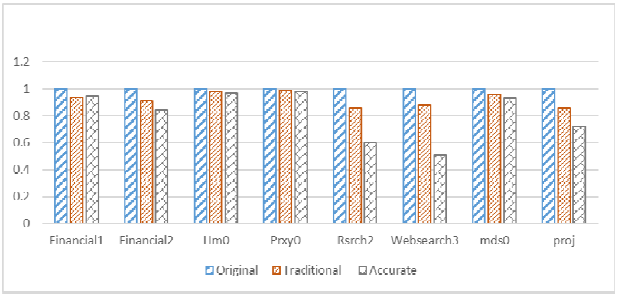

Figure 5. Normalized average response time

Average response delay optimization:

Figure 6 shows the normalized refresh times of the traditional refresh strategy and the precise refresh strategy. Compared with the traditional refresh strategy, the refresh volume of the precise refresh strategy is reduced by 12% to 58%. Although the average response time optimization effect of financial1, prxy0, and other workloads is not obvious. However, the number of refreshes is significantly reduced, and under the same conditions, the service life of the flash memory storage device is prolonged.

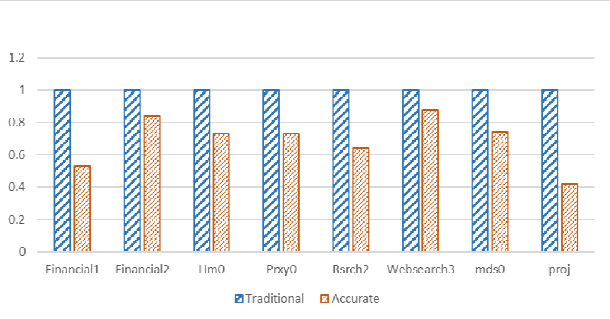

Figure 6. Normalized refresh times

V. CONCLUSION

With the advancement of storage technology and the increase in the density of flash memory devices, the reliability of flash memory has declined. Using data refresh operation can increase the reliability of flash memory and improve the read and write performance of flash memory storage devices. However, frequent refresh operations will further damage the performance and lifetime of the flash memory. Therefore, we have proposed a precise refresh strategy to refresh only the data that needs to be refreshed, which reduces the wear of the flash memory device and improves the reading efficiency.

VI. ACKNOWLEDGEMENT

This work is supported by The National Natural Science Foundation of China under Grant No.61762075. It is also supported by The Provincial Nature Science Foundation of Qinghai under Grant No.2020-ZJ-926. Ping Xie is the corresponding author of this paper.

REFERENCES

[1] Cernea, R. A., Pham, L., Moogat, F., Chan, S., Le, B., Li, Y., ... & Quader, K. (2008). A 34 MB/s MLC write throughput 16 Gb NAND with all bit line architecture on 56 nm technology. IEEE Journal of Solid-State Circuits, 44(1), 186-194.

[2] Tokutomi, T., Tanakamaru, S., Iwasaki, T. O., & Takeuchi, K. (2014, May). Advanced error prediction LDPC for high-speed reliable TLC nand-based SSDs. In 2014 IEEE 6th International Memory Workshop (IMW) (pp. 1-4). IEEE.

[3] Zhao, K., Zhao, W., Sun, H., Zhang, X., Zheng, N., & Zhang, T. (2013). LDPC-in-SSD: Making advanced error correction codes work effectively in solid state drives. In 11th {USENIX} Conference on File and Storage Technologies ({FAST} 13) (pp. 243-256).

[4] Tanakamaru, S., Yanagihara, Y., & Takeuchi, K. (2013, January). Highly reliable solid-state drives (SSDs) with error-prediction LDPC (EP-LDPC) architecture and error-recovery scheme. In 2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC) (pp. 83-84). IEEE.

[5] Liu, R. S., Chuang, M. Y., Yang, C. L., Li, C. H., Ho, K. C., & Li, H. P. (2014, June). EC-Cache: Exploiting error locality to optimize LDPC in NAND flash-based SSDs. In 2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC) (pp. 1-6). IEEE.

[6] Du, Y., Zou, D., Li, Q., Shi, L., Jin, H., & Xue, C. J. (2017, May). Laldpc: Latency-aware ldpc for read performance improvement of solid state drives. In Proc. MSST (pp. 1-11).

[7] Cai, Y., Yalcin, G., Mutlu, O., Haratsch, E. F., Cristal, A., Unsal, O. S., & Mai, K. (2012, September). Flash correct-and-refresh: Retention-aware error management for increased flash memory lifetime. In 2012 IEEE 30th International Conference on Computer Design (ICCD) (pp. 94-101). IEEE.

[8] Lv, Y., Shi, L., Li, Q., Gao, C., Xue, C. J., & Sha, E. (2019, August). Optimizing Tail Latency of LDPC based Flash Memory Storage Systems Via Smart Refresh. In 2019 IEEE International Conference on Networking, Architecture and Storage (NAS) (pp. 1-8). IEEE.

[9] Ryan, W. E. (2004). An introduction to LDPC codes. CRC Handbook for Coding and Signal Processing for Recording Systems, 1-23.

[10] Van Houdt, B. (2013). Performance of garbage collection algorithms for flash-based solid state drives with hot/cold data. Performance Evaluation, 70(10), 692-703.

[11] Zhou, B., Wan, S., & Xie, C. (2021). Isolation: Inexpensively separating cold data via garbage collection to improve the lifetime and performance of NAND flash SSDs. Concurrency and Computation: Practice and Experience, 33(15), e5460.

[12] Hwang, S. H., Kwak, J. W., & Park, C. H. (2015). Cold Data Identification using Raw Bit Error Rate in Wear Leveling for NAND Flash Memory. Journal of the Korea Society of Computer and Information, 20(12), 1-8.

[13] Luo, Y., Cai, Y., Ghose, S., Choi, J., & Mutlu, O. (2015, May). WARM: Improving NAND flash memory lifetime with write-hotness aware retention management. In 2015 31st Symposium on Mass Storage Systems and Technologies (MSST) (pp. 1-14). IEEE.

[14] Bucy, J. S., & Ganger, G. R. (2003). The DiskSim simulation environment version 3.0 reference manual. School of Computer Science, Carnegie Mellon University.